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- <u>L5</u> L1 same bus same speed
- L4 L1 same bus
- L3 L1 and "variable speed bus"
- <u>L2</u> L1 same "variable speed bus"
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- L5 L1 same bus same speed
- L4 L1 same bus
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- L2 L1 same "variable speed bus"
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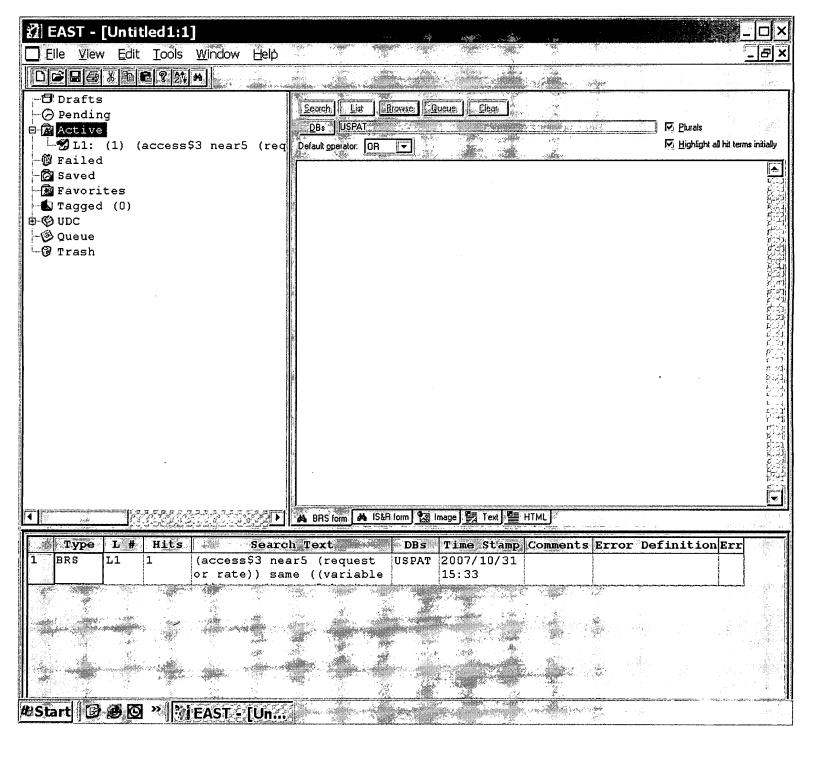
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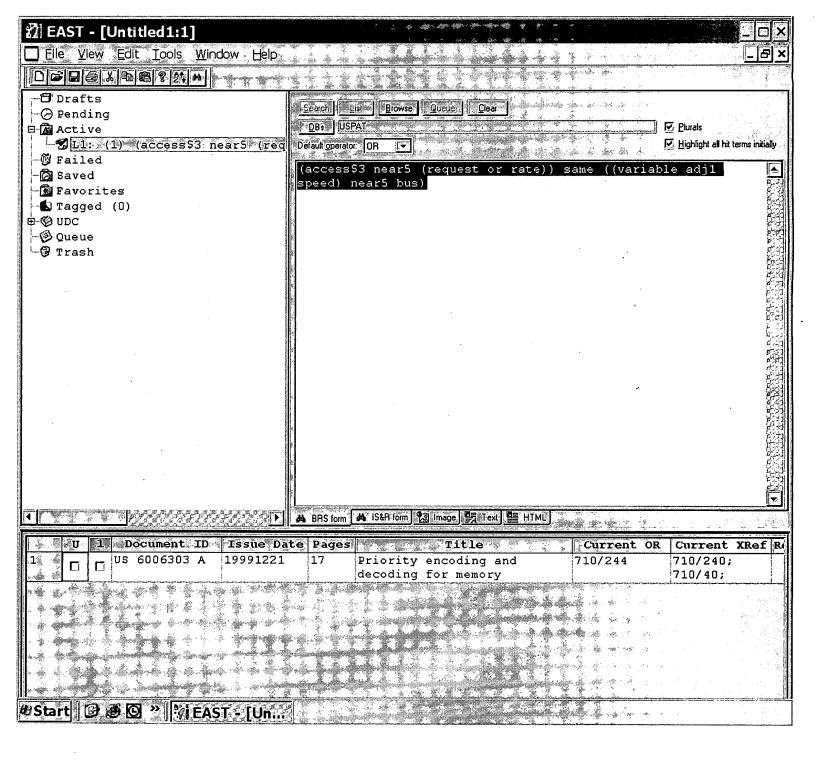
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- L6 L1 same bus same (variable near3 speed)
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IEEE STD	IEEE Standard	Digital Object Identifier 10.1109/12.895938 AbstractPlus References Full Text: PDF(376 KB) IEEE JNL				
		Rights and Permissions 2. On the nature and inadequacies of transport timing delay constructs in Vermissions Walker, P.A.; Ghosh, S.;				
		Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction Volume 16, Issue 8, Aug. 1997 Page(s):894 - 915 Digital Object Identifier 10.1109/43.644615				
		AbstractPlus References Full Text: PDF(472 KB) IEEE JNL Rights and Permissions				
		3. A novel 2 GHz multi-layer AMBA high-speed bus interconnect matrix for Landry, A.; Nekili, M.; Savaria, Y.; Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on 23-26 May 2005 Page(s):3343 - 3346 Vol. 4 Digital Object Identifier 10.1109/ISCAS.2005.1465344				
		AbstractPlus Full Text: PDF(264 KB) IEEE CNF Rights and Permissions				
		4. Eliminating non-determinism during test of high-speed source synchron buses Mohanram, K.; Touba, N.A.; VLSI Test Symposium, 2003. Proceedings. 21st 27 April-1 May 2003 Page(s):121 - 127				
		AbstractPlus Full Text: PDF(347 KB) IEEE CNF Rights and Permissions				
		5. A signalling system for multiprocessors				

Prete, C.A.; Rizzo, L.;

13-16 May 1991 Page(s):358 - 362

CompEuro '91. 'Advanced Computer Technology, Reliable Systems and Applic

Annual European Computer Conference. Proceedings.

Digital Object Identifier 10.1109/CMPEUR.1991.257410 AbstractPlus | Full Text: PDF(464 KB) | IEEE CNF Rights and Permissions - 6. A dynamic high speed multi-media local area network (MLAN) protocol at Agrawal, J.P.; Varshney, U.; Military Communications Conference, 1992. MILCOM '92, Conference Record. - Fusing Command, Control and Intelligence'., IEEE 11-14 Oct. 1992 Page(s):1011 - 1015 vol.3 Digital Object Identifier 10.1109/MILCOM.1992.243956 AbstractPlus | Full Text: PDF(496 KB) IEEE CNF Rights and Permissions 7. CADRE: Cycle-Accurate Deterministic Replay for Hardware Debugging Sarangi, S.R.; Greskamp, B.; Torrellas, J.; Dependable Systems and Networks, 2006. DSN 2006. International Conference 2006 Page(s):301 - 312 Digital Object Identifier 10.1109/DSN.2006.19 AbstractPlus | Full Text: PDF(406 KB) IEEE CNF Rights and Permissions 8. A mixed EFL I²L digital telecommunication integrated circuit П Baumert, R.J.; Cameron, L.E.; Wilson, R.A., III; Electron Devices, IEEE Transactions on Volume 31, Issue 2, Feb 1984 Page(s):160 - 165 AbstractPlus | Full Text: PDF(760 KB) IEEE JNL Rights and Permissions 9. A mixed EFL/I/SUP 2/L digital telecommunication integrated circuit Baumert, R.J.; Cameron, L.E., III; Wilson, R.A.; Solid-State Circuits, IEEE Journal of Volume 19, Issue 1, Feb 1984 Page(s):26 - 31 AbstractPlus | Full Text: PDF(992 KB) | IEEE JNL Rights and Permissions 10. A process-independent, 800-MB/s, DRAM byte-wide interface featuring co interleaving and concurrent memory operation Griffin, M.M.; Zerbe, J.; Tsang, G.; Ching, M.; Portmann, C.L.; Solid-State Circuits, IEEE Journal of Volume 33, Issue 11, Nov. 1998 Page(s):1741 - 1751 Digital Object Identifier 10.1109/4.726569 AbstractPlus | References | Full Text: PDF(344 KB) | IEEE JNL Rights and Permissions 11. An architecture and compiler for scalable on-chip communication П Jian Liang; Laffely, A.; Srinivasan, S.; Tessier, R.; Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Volume 12, Issue 7, July 2004 Page(s):711 - 726 Digital Object Identifier 10.1109/TVLSI.2004.830919 AbstractPlus | References | Full Text: PDF(1472 KB) | IEEE JNL Rights and Permissions 12. High-Speed FPGA-Based Pulse-Height Analyzer for High Resolution X-R: Buzzetti, S.; Capou, M.; Guazzoni, C.; Longoni, A.; Mariani, R.; Moser, S.; Nuclear Science, IEEE Transactions on Volume 52, <u>Issue 4</u>, Aug. 2005 Page(s):854 - 860 Digital Object Identifier 10.1109/TNS.2005.852699 AbstractPlus | Full Text: PDF(616 KB) | IEEE JNL

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13. Wide dynamic range, high-speed machine vision with a 2Ã2256 pixel tem vision sensor Posch, C.; Hofstatter, M.; Litzenberger, M.; Matolin, D.; Donath, N.; Schon, P.; Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on 27-30 May 2007 Page(s):1196 - 1199 Digital Object Identifier 10.1109/ISCAS.2007.378266 AbstractPlus | Full Text: PDF(1330 KB) IEEE CNF Rights and Permissions 14. An Application Specific Processor for Montecarlo Simulations Danese, G.; Leporati, F.; Bera, M.; Giachero, M.; Nazzicari, N.; Spelgatti, A.; Parallel, Distributed and Network-Based Processing, 2007. PDP '07, 15th EUF International Conference on 7-9 Feb. 2007 Page(s):262 - 269 Digital Object Identifier 10.1109/PDP.2007.21 AbstractPlus | Full Text: PDF(295 KB) | IEEE CNF Rights and Permissions 15. A Fault-Tolerant Dynamic Fetch Policy for SMT Processors in Multi-Bus I Fechner, B.; Parallel Computing in Electrical Engineering, 2006. PAR ELEC 2006. International Computing in Electrical Engineering, 2006. 2006 Page(s):31 - 36 Digital Object Identifier 10.1109/PARELEC.2006.4 AbstractPlus | Full Text: PDF(131 KB) IEEE CNF Rights and Permissions 16. Modeling and analysis of high-speed links Stojanovic, V.; Horowitz, M.; Custom Integrated Circuits Conference, 2003. Proceedings of the IEEE 2003 21-24 Sept. 2003 Page(s):589 - 594 Digital Object Identifier 10.1109/CICC.2003.1249467 AbstractPlus | Full Text: PDF(464 KB) IEEE CNF Rights and Permissions 17. Design of a Firewire based data acquisition system for use in animal PE1 Lewellen, T.K.; Laymon, C.M.; Miyaoka, R.S.; Ki Sung Lee; Kinahan, P.E.; Nuclear Science Symposium Conference Record, 2001 IEEE Volume 4, 4-10 Nov. 2001 Page(s):1974 - 1978 Digital Object Identifier 10.1109/NSSMIC.2001.1009211 AbstractPlus | Full Text: PDF(267 KB) IEEE CNF Rights and Permissions 18. Debugging aids for systems-on-a-chip Bannatyne, R.; Northcon/98 Conference Proceedings 21-23 Oct. 1998 Page(s):159 - 163 Digital Object Identifier 10.1109/NORTHC.1998.731528 AbstractPlus | Full Text: PDF(348 KB) IEEE CNF Rights and Permissions

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